C of C

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 7,177,196	)	Serial No. 10/073,999
Inventor(s): Ken TAKEUCHI *et al*	)	Filed: February 14, 2002
Issue Date: February 13, 2007	)	Attorney Docket No. 001701.00140

For: NONVOLATILE SEMICONDUCTOR MEMORY HAVING PLURAL DATA STORAGE PORTIONS FOR A BIT LINE CONNECTED TO MEMORY CELLS

REQUEST FOR CERTIFICATE OF CORRECTION

U.S. Patent and Trademark Office
Customer Service Window
Randolph Building, Mail Stop: Certificate of Correction Branch
401 Dulany Street
Alexandria, VA 22314

Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322, this is a request for the issuance of a Certificate of Correction in the above-identified patent. Two (2) copies of PTO Form 1050 are appended. The complete Certificate of Correction involves one page.

The mistakes identified in the appended Form occurred through no fault of the Applicants, as clearly disclosed by the records of the application, which matured into this patent. Enclosed for your convenience are the relevant portions of the Amendment filed July 31, 2006.

Issuance of the Certificate of Correction containing the corrections is respectfully requested. Since these changes are necessitated through no fault of the Applicants, no fee is believed to be associated with this request. Nonetheless, should the Patent and Trademark Office determine that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

By: _____
Christopher R. Glembocki
Registration No. 38,800

Dated: September 12, 2007
Banner & Witcoff, Ltd
1100 13th Street, N.W., Suite 1200
Washington, D.C. 20005-4051
(202) 824-3000

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 7,177,196

DATED: February 13, 2007

INVENTOR(S): Ken TAKEUCHI *et al*

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the cover page, References Cited section (56), Foreign Patent Documents:
Please insert the following references:

--JP	11-17619	07/1999
JP	11-167800	06/1999
CN	1211040A	03/1999--

In Column 101, Claim 5, Line 1:
Please replace "bit connected" with --bit line connected--

In Column 101, Claim 5, Line 21:
Please replace "second memory cell" with --second bit line is latched in said common latch circuit and a verify read operation to verify whether said second memory cell--

In Column 101, Claim 10, Line 59:
Please insert --a second bit line;--

In Claim 11, Column 102, Line 31-Column 103, Line 4:
Please replace Claim 11 with the following:
--The nonvolatile semiconductor memory according to claim 10, wherein said first and second memory cells are connected to a same word line.--

In Claim 12, Column 102, Lines 5-8:
Please replace Claim 12 with the following:
--The nonvolatile semiconductor memory according to claim 11, wherein while said program/read data is held by said first, second, third, or fourth bit line, a potential of a bit line adjacent to said first, second, third, or fourth bit line is set at a fixed potential.--

In Claim 13, Column 104, Lines 1-6:
Please replace --The nonvolatile semiconductor memory according to claim 12, wherein said fixed potential is a ground potential or a power supply potential.--

Mailing Address of Sender:

Banner & Witcoff, Ltd.
11th Floor
1001 G Street, N.W.
Washington, DC 20001-4597

FORM PTO 1050 (Rev.2-93)

U.S. PAT. NO 7,177,196

No. of add'l copies
@ $0.50 per page

SEP 25 2007

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 7,177,196

DATED: February 13, 2007

INVENTOR(S): Ken TAKEUCHI *et al*

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In Claim 12, Column 102, Lines 5-8:
Please replace Claim 12 with the following:
--The nonvolatile semiconductor memory according to claim 11, wherein while said program/read data is held by said first, second, third, or fourth bit line, a potential of a bit line adjacent to said first, second, third, or fourth bit line is set at a fixed potential.--

In Claim 13, Column 104, Lines 1-6:
Please replace --The nonvolatile semiconductor memory according to claim 12, wherein said fixed potential is a ground potential or a power supply potential.--

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Washington, DC 20001-4597

FORM PTO 1050 (Rev.2-93)

U.S. PAT. NO 7,177,196

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SEP 25 2007

Acknowledgement Receipt

The USPTO has received your submission at **14:05:18** Eastern Time on **31-JUL-2006** .

No fees have been paid for this submission. Please remember to pay any required fees on time to prevent abandonment of your application.

eFiled Application Information

EFS ID	1133677
Application Number	10073999
Confirmation Number	9741
Title	NONVOLATILE SEMICONDUCTOR MEMORY HAVING PLURAL DATA STORAGE PORTIONS FOR A BIT LINE CONNECTED TO MEMORY CELLS
First Named Inventor	Ken Takeuchi
Customer Number or Correspondence Address	22907
Filed By	Christopher R. Glembocki
Attorney Docket Number	001701.00140
Filing Date	14-FEB-2002
Receipt Date	31-JUL-2006
Application Type	Utility

Application Details

Submitted Files	Page Count	Document Description	File Size	Warnings
001701_00140_amend_07_31_2006.pdf	6		89003 bytes	PASS

Document Description	Page Start	Page End
Amendment - After Non-Final Rejection	1	1
Claims	2	5
Applicant Arguments/Remarks Made in an Amendment	6	6

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance

of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

If you need help:

- *Call the Patent Electronic Business Center at (866) 217-9197 (toll free) or e-mail EBC@uspto.gov for specific questions about Patent e-Filing.*
- *Send general questions about USPTO programs to the USPTO Contact Center (UCC) .*
- *If you experience technical difficulties or problems with this application, please report them via e-mail to Electronic Business Support or call 1 800-786-9199.*

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application Of	)		
	)	Group Art Unit:	2827
Ken Takeuchi et al.	)		
	)	Examiner:	H. Ho
Serial No.: 10/073,999	)		
	)		
Filed: February 14, 2002	)	Confirmation No.	9741
	)		
For: Nonvolatile Semiconductor Memory Having Plural Data Storage Portions For A Bit Line Connected To Memory Cells	)	Atty.. No.	001701.00140

U.S. Patent and Trademark Office
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Amendment

The paper is being filed in response to the office action of July 28, 2006. If any fees are required for this paper, please charge such fees to deposit account no. 19-0733.

Listing of Claims begins on page 2 of this paper.

Remarks begin on page 6 of this paper.

The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1 – 47. Cancelled

48. (Currently Amended) A nonvolatile semiconductor memory comprising:

a first string line including a first memory cell and a first select transistor connected in series;

a second string line including a second memory cell and a second select transistor connected in series;

a first bit line connected to said first string line;

a second bit line connected to said second string line, being different from said first bit line;

a common node connected to one ends of said first and second bit lines; and

a common latch circuit connected to said common node,

wherein

said first and second memory cells are programmed substantially simultaneously; and

while ~~said~~ a program voltage is supplied to said second memory cell, a verify read operation to verify whether said first memory cell has been programmed sufficiently, is carried out by said common latch circuit, and while said program voltage is supplied to said first memory cell, a verify read operation to verify whether said second memory cell has been programmed sufficiently, is carried out by said latch common circuit.

49. (Currently Amended) A nonvolatile semiconductor memory according to claim 48, wherein

while ~~a~~ said program voltage is supplied to said second memory cell, program data of said second memory cell is held by said second bit line, and

while said program voltage is supplied to said first memory cell, program data of said first memory cell is held by said first bit line.

50. (Previously Presented) A nonvolatile semiconductor memory comprising:

a first string line including a first memory cell and a first select transistor connected in series;

a second string line including a second memory cell and a second select transistor connected in series;

a first bit line connected to said first string line;

a second bit line connected to said second string line, being different from said first bit line;

a common node connected to one ends of said first and second bit lines; and

a common latch circuit connected to said common node,

wherein

said first and second memory cells are programmed substantially simultaneously;

while a program voltage is supplied to said second memory cell, program data of said second memory cell is held by said second bit line, and while said program voltage is supplied to said second memory cell, the program data of said first memory cell held by said first bit line is latched in said common latch circuit and a verify read operation to verify whether said first memory cell has been programmed sufficiently, is carried out by said common latch circuit;

while said program voltage is supplied to said first memory cell, program data of said first memory cell is held by said first bit line, and while said program voltage is supplied to said first memory cell, the program of data said second memory cell held by said second bit line is latched in said common latch circuit and a verify read operation to verify whether said second memory cell has been programmed sufficiently, is carried out by said common latch circuit.

51. Cancelled.

52. (Original) The nonvolatile semiconductor memory according to claim 48, wherein said first memory cell and said second memory cell are connected to different word lines.

53. (Original) The nonvolatile semiconductor memory according to claim 49, wherein said first memory cell and said second memory cell are connected to different word lines.

54. (Original) The nonvolatile semiconductor memory according to claim 50, wherein said first memory cell and said second memory cell are connected to different word lines.

55. Cancelled.

56. (Previously Presented) A nonvolatile semiconductor memory comprising:

a first string line including a first memory cell and a first select transistor connected in series;

a first bit line connected to said first string line;

a second bit line, being different from said first bit line;

a common node connected to one ends of said first and second bit lines latching program / read data; and

a common latch circuit connected to said common node,

wherein

while a program voltage is supplied to said first memory cell, program data of said first memory cell is held by at least one of said first and second bit lines;

after said program voltage is supplied to said first memory cell, said common latch circuit is electrically connected to said second bit line and the program data of said first memory cell held by said second bit line is latched in said common latch circuit; and

a verify read operation to verify whether said first memory cell has been sufficiently programmed, is carried out using said program data latched in said common latch circuit.

57. (Previously Presented) A nonvolatile semiconductor memory comprising:

a first string line including a first memory cell and a first select transistor connected in series;

a first bit line connected to said first string line;

a second bit line;

a second string line including a second memory cell and a second select transistor connected in series;

a third bit line connected to said second string line;

a fourth bit line;

a common node connected to one ends of said first, second, third and fourth bit lines, latching program/read data of at least one of said first and second memory cells; and

a common latch circuit connected to said common node,

wherein

said first, second, third and fourth bit lines are different from each other;

said first and second memory cells are programmed substantially simultaneously, program data of said first memory cell is held by at least one of said first and second bit lines, and program data of said second memory cell is held by at least one of said third and fourth bit lines while a program voltage is supplied to said first and second memory cells;

a verify read operation to verify whether said first memory cell has been sufficiently

programmed, is carried out by said common latch circuit, and program data of said second memory cell is held by said fourth bit line while conducting the verify read operation of said first memory cell; and

said common latch circuit and said fourth bit line are electrically connected to each other, after the program data of said second memory cell held by said fourth bit line is latched in said common latch circuit, a verify read operation to verify whether said second memory cell has been sufficiently programmed, is carried out using the program data of said second memory cell held by said common latch circuit, and while conducting a verify read operation of said second memory cell, the program data of said first memory cell is held by said second bit line.

58. (Previously Presented) The nonvolatile semiconductor memory according to claim 57, wherein

said first and second memory cells are connected to a same word line.

59 - 61. Cancelled.

62. (Previously Presented) The nonvolatile semiconductor memory according to claim 56, wherein

while said program / read data is held by said first or second bit line, a potential of a bit line adjacent to said first or second bit line is set at a fixed potential.

63. (Original) The nonvolatile semiconductor memory according to claim 62, wherein said fixed potential is a ground potential or a power supply potential.

64. Canceled

65. (Previously Presented) The nonvolatile semiconductor memory according to claim 57, wherein

while said program / read data is held by said first, second, third or fourth bit line, a potential of a bit line adjacent to said first, second, third or fourth bit line is set at a fixed potential.

66. (Previously Presented) The nonvolatile semiconductor memory according to claim 65, wherein said fixed potential is a ground potential or a power supply potential.

67-81. Canceled

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,999	02/14/2002	Ken Takeuchi	001701.00140	9741

22907 7590 04/14/2005

BANNER & WITCOFF
1001 G STREET N W
SUITE 1100
WASHINGTON, DC 20001

EXAMINER	
HO, HOAI V	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SEP 25 2007

EJ

Office Action Summary	Application No.	Applicant(s)
	10/073,999	TAKEUCHI ET AL.
	Examiner	Art Unit
	Hoai V. Ho	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/23/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-60,62,63,65 and 66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47-60,62,63,65 and 66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/667,610.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/10/05*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

SEP 25 2007

PTO/SB/08a (08-03)
Approved for use through 07/31/2003. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete If Known	
Application Number	10/073,9999
Filing Date	February 14, 2002
First Named Inventor	Ken Takeuchi et al.
Art Unit	~~2818~~ 2827
Examiner Name	H. Ho
Attorney Docket Number	001701.00140

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] - Number[4] - Kind Code[5]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
[illegible]		JP 11-17619	07/02/1999	Lee Jin-Woo et al.		Abstract
[illegible]		JP 11-167800	06/22/1999	Kanda Kazue		Abstract
[illegible]		CN 1211040A	03/17/1999	Chung D. J. et al.		Abstract

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Chinese Office Action with translation.	YES

Examiner Signature	H. Ho	Date Considered	March 31, 2005

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.